PATENT
Customer No. 22,852
Attorney Docket No. 06720.0086-01000

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Chyh-Yih CHANG	Parent Group Art Unit: 2811
1.53(b) Divisional of Appl. No. 10/138,405, filed May 6, 2002	Parent Examiner: Nadav, O.
Filed: Herewith	
For: BI-DIRECTIONAL SILICON CONTROLLED RECTIFIER FOR ELECTROSTATIC DISCHARGE PROTECTION	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicant brings to the attention of the Office the documents listed on the attached PTO form 1449. This Information Disclosure Statement is being filed together with this Divisional application.

Copies of the listed documents were previously submitted in a prior application, application no. 10/138,405, filing date May 6, 2002, upon which applicant relies for the benefits provided in 35 U.S.C. § 120. Applicant respectfully requests that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

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This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Office applies any of the documents as prior art against any claim in the application and Applicant determines that the cited documents do not constitute "prior art" under United States law, Applicant reserves the right to present to the Office the relevant facts and law regarding the appropriate status of such documents.

Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 25, 2003

By: Robert F. Rotella Reg 24,014
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OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,258,634	07/10/2001	Wang et al.			
		5,910,874	06/08/1999	Iniewski et al.			
		5,646,808	07/08/1997	Nakayama			
		5,519,242	05/21/1996	Avery			
		5,631,793	05/20/1997	Ker et al.			
		5,811,857	09/22/1998	Assaderaghi et al.			
		5,502,328	03/26/96	Chen et al.			
		5,581,104	12/03/96	Lowrey et al.			
		5,990,520	11/23/99	Noorlag et al.			
FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
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		5,907,462	05/25/99	Chatterjee et al.			
		5,932,918	08/03/99	Krakauer			
		6,015,992	01/18/00	Chatterjee et al.			
		5,453,384	09/26/95	Chatterjee			

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		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	N. K. Verghese and D. Allstot, "Verification of RF and Mixed-Signed Integrated Circuits for Substrate Coupling Effects", in *Proc. of IEEE Custom Integrated Circuits Conf.*, 1997, pp. 363-370
	M.Xu, D. Su, D. Shaeffer, T.Lee, and B. Wooley, "Measuring and Modeling the Effects of Substrate Noise on LNA for a CMOS GPS Receiver, "*IEEE Journal of Solid-State Circuits*, vol. 36, pp. 473-485, 2001.
	R. Gharpurey, "A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits," in *Proc. of IEEE Custom Integrated Circuits Conf.*, 1999, pp. 487-490.
	M. Nagata, J. Nagai, K. Hijikata, T. Morie, and A. Iwata, "PhysicalDesign Guides for Substate Noise Reduction in CMOS Digital Circuits, "*IEEE Journal of Solid-State Circuits*, vol. 36, pp. 539-549, 2001.
	M.-D. Ker, T-Y, Chen, C-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin WIth Very Low Input Capacitance for High-Frequency or Current-Mode Applications, "*IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1194-1199, 2000.
	M.-D. Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuit for Submicron CMOS VLSI, "*IEEE Trans. on Electron Devices*, vol. 46, pp. 173-183, 1999

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Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,081,002	06/27/2000	Amerasekera et al			
		5,754,381	05/19/1998	Ker			
		5,465,189	11/07/1995	Polgreen et al.			
		5,225,702	07/06/1993	Chatterjee			
		5,012,317	04/30/1991	Rountre			
		4,939,616	07/03/1990	Rountree			

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on Different ESD Protection Strategies Devoted to 3.3V RF Applications (2 (GHz) in a 0.18μm CMOS Process, "in Proc. of EOS/ESD Symp., 200, pp. 251-259.
	T.-Y. Chen and M.-D. Ker, "Design on ESD Protection Circuit With Low and Constant Input Capacitance," *in Proc. of IEEE Int. Symp. on Quality Electronic Design, 2001*, pp. 247-247.
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		5,629,544	05/13/97	Voldman et al.			
		6,034,397	03/07/00	Voldman			
		5,940,258	08/17/99	Duvvury			
		5,807,791	09/15/98	Bertin et al			
		5,719,737	02/17/98	Maloney			
		5,654,862	08/05/97	Worley et al.			

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	S.Voldman, et al. , "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon- Bound Source/Drain Diodes for ESD Networks," in Proc. of EOS/ESD Symp., 1998, pp. 151-160
	S. Voldman, et al., "Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors," in Proc. of EOS/ESD symposium, 1995, pp. 43-61.
	M.J. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol.30, no. 7, pp.823-825, July 1995.
	G.P. Singh, et al., "High-Voltage-Tolerant I/OBuffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol.34, no. 11, pp. 1512-1525, Nov. 1999.
	H. Sanchez, et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in 02. -μm, 3.5-nm Tox, 1.8 -V CMOS Technology, " IEEE Journal of Solid-State Circuits, vol.34 no. 11.pp. 1501-1511, Nov. 1999

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